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Implementation of High Performance Fir Filter Using Low Power Multiplier and Adder

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ABSTRACT
The ever increasing growth in laptop and portable systems in cellular networks has intensified the research efforts in low power microelectronics. Now a day, there are many portable applications requiring low power and high throughput than ever before. Thus, low power system design has become a significant performance goal. So this paper is face with more constraints: high speed, high throughput, and at the same time, consumes as minimal power as possible. The Finite Impulse Response (FIR) Filter is the important component for designing an efficient digital signal processing system. So, in this paper author trying, a FIR filter is constructing, which is efficient not only in terms of power and speed but also in terms of delay. When consider the elementary structure of an FIR filter, it is found that it is a combination of multipliers and delays, which in turn are the combination of adders. . This paper presents an efficient implementation and analysis for performance evaluation of multiplier and adder to minimize the consumption of energy during multiplication and addition methodology to improve the performance by compares different type of Multipliers and adder, respectively. By using, power comparison result of adders and multiplier, choice low power adder and multiplier to implementation of high performance FIR filter.
Keywords *– DSP, FPGA, Multiplier, VHDL*

I. INTRODUCTION

In today scenario low power consumption and smaller area are the most important parameter for the fabrication of DSP systems and high performance systems. To save notable power consumption of a DSP system, it is good to reduce its dynamic power that is the important part of total power dissipation. Digital filter are essential elements of DSP system. Digital filter can be realized by different digital filter structure such as direct form-I & II, transposed structure etc. These structures provide a space for selection of appropriate structure for minimizing of power consumption and improvement in speed of digital filter which is play important role in all high performance DSP applications.[4] FIR filter and IIR filter are two types of Digital filter. FIR filter mostly pefer over IIR filter due to its linear phase characteristics, low coefficient sensitivity, guarantee stability.

Multiplication and addition occurs frequently in 'Finite Impulse Response' (FIR). In FIR filter, multiplier and adder plays an important role. A multiplier in a FIR filter is most power consumption component. Multiply and Accumulate (MAC) is an important unit of DSP system. It decides the power consumption and speed of operation of DSP system. Most of DSP consumption involve the use of multiplier accumulate operation and therefore the design of fast and efficient multiplier imperative. . The dynamic switching power consumption of digital FIR filter is reduced by using data transition power diminution technique. This technique is used on adder, multiplier and applied for filters to remove power consumption caused by unwanted data transmission.

II. FIR FILTER THEORY

Finite Impulse Response (FIR) filter are type of digital filter and consist of weighting sequence (impulse response) among non-recursive digital filters which is finite in length. FIR filters are non-recursive digital filters has been selected for this thesis due to their good characteristics.[4] FIR filter has no feedback and its input-output relation is given by

$$y[n] = \sum_{k=0}^{N-1} a[k] \, . \, x[n-k]$$

Here, x [n] and y [n] are the filter input and filter output respectively, a [k] is the filter coefficients, N is the filter coefficient number.

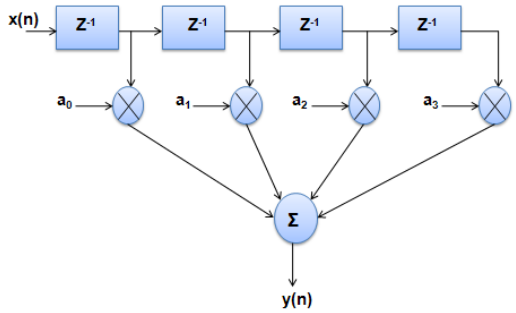

Fig. 1: FIR Filter

As shown in figure output y [n] of a FIR filter is a function only of the input signal x [n]. The response of such a filter to an impulse consists of a finite sequence of N+1 samples, where N is the filter order.

III. DIGITAL ADDERS

3.1 RIPPLE CARRY ADDER

A simple Ripple Carry Adder (RCA)is type of adder used in digital circuit. It creates the addition of two binary numbers. It is constructed by cascading connection of full adder in series. The carry output of first full adder ripple to the carry input of the next full adder in the chain.

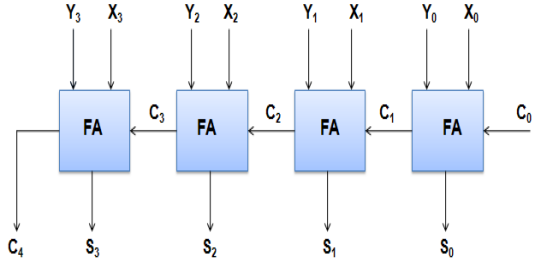

Fig 2: Ripple Carry Adder

3.2 CARRY LOOK AHEAD ADDER

A Carry-Look Ahead Adder (CLA) improves speed by reducing the computation time required to determine carry bits. The CLA compute all carry bits before the sum, which decrease the delay time to calculate the result of the larger value bits. The CLA solves the carry delay problem by predetermine the carry signals in advance basis of the input signals.

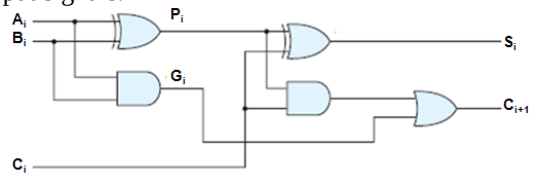

Fig. 3: Carry Look Ahead Generator

Ai and Bi are data input of bit i of an adder cell, and C_i is its carry input. C_{i+1} are the carry output and Si is the sum.

$$C_{i+1} = G_i \text{ or } P_i\ C_i$$
$$S_i = P_i \text{ xor } C_i$$

here,

$$G_i = A_i \text{ and } B_i$$
$$P_i = A_i \text{ xor } B_i$$

Pi and Gi are known as the carry generate and carry propagate terms, respectively.

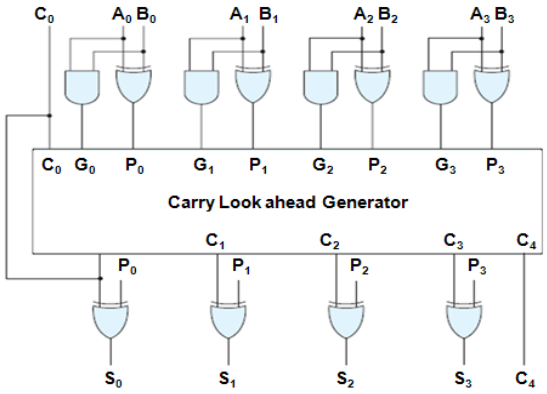

Fig. 4: Carry Look Ahead Adder

3.3 CARRY SELECT ADDER

A Carry Select Adder us a logic element that evaluate the (n+1) bit addition of two n-bit numbers. The carry select adder usually includes two ripple carry adder and a multiplexer. Sum of two n-bit numbers with a carry select adder is done by using two adders (therefore two ripple carry adders) in order to perform the adding up twice, one tie with the appropriation of the carry existence zero and the other assuming one.

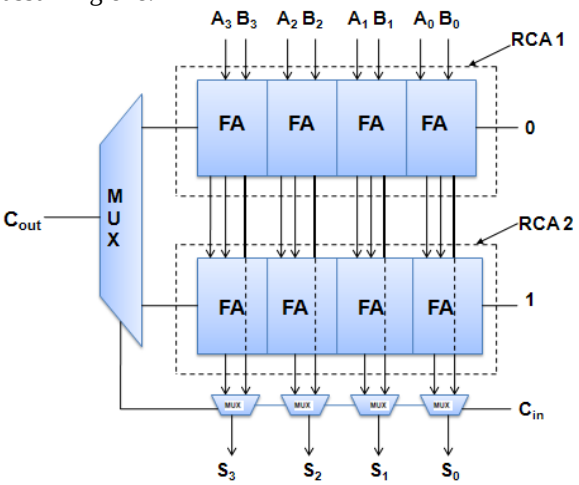

Fig. 5: Carry Select Adder

3.3 CARRY SAVE ADDER

A Carry Save Adder (CSA) is type of digital adder with low carry signal propagation delay, but in place of adding two input numbers to a single sum output, it adds three input numbers to an output pair of numbers. When its two outputs are then summed

by using a carry-look ahead or ripple-carry adder, we obtain the sum of all three inputs.

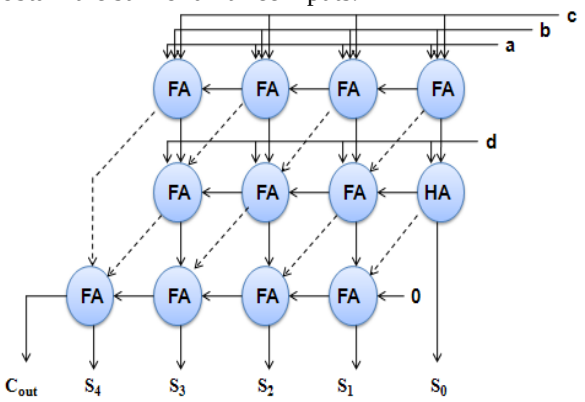

Fig. 6: Carry Save Adder

IV. DIGITAL MULTIPLIER

4.1 ARRAY MULTIPLIER

Array multiplier is type of combination multiplier, in which combinational n*n multiplier involve an array on n*n multiplier cells each of which is important for multiplying a bit of multiplier with a bit of multiplicand and summing the result with the product bit being from a previous multiplication stage.

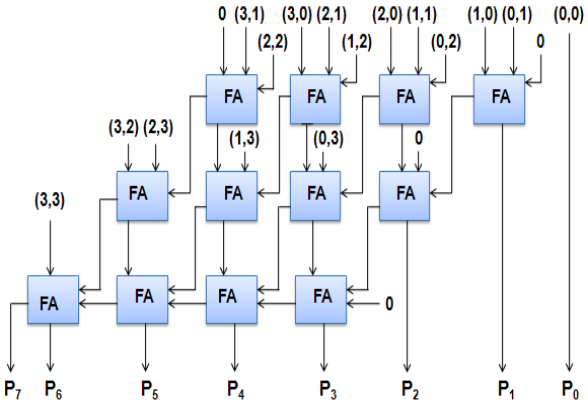

Fig. 7: Array Multiplier

4.2 RADIX-2 BOOTH MULTIPLIER

This is technique that allows for smaller, faster multiplication circuits by recoding the numbers that are multiplied. It allows only half of product which is needed during computation that is no. of partial products is reduced by factor 2.

4.2.1 RADIX-2 BOOTH ALGORITHM

The Booth's algorithm is for multiplying binary signed number in 2's complement. Let the multiplicand and multiplier represent by R and M, respectively; and let n and q represent the number of bits in R and M. Take the 2's complement of R which known as –R. For calculation, make the table of A, B, R and R-1 variable, respectively.

Step1:

a) Fill M value in the table.
b) Fill 0 for M-1 value it should be the previous first least significant bit of M.
c) Fill 0 in A and B rows which show the product of M and R at the end of multiplication operation.
d) Take n rows for every cycle; this is because we are multiplying n bits numbers.

Step2:

Booth algorithm requires evaluation of the multiplier bits, and shifting of the partial product.

Use the first least significant bits of the multiplier "M", and the previous least significant bits of the multiplier "M - 1" to determine the arithmetic action.

a) Determine the two least significant (right most) bits of M.
   1. If they are 00, no change.
   2. If they are 11, no change.
   3. If they are 01, add R+A.
   4. If they are 10, add (-R)+A.

   Arithmetically shift the value calculate in step1-4 by signal place of right.
b) Take A & B together and arithmetically right shift which store the sign bit of 2's complement number. Hence a positive number and a negative number remains unchanged.
c) Right shift circulate M due to this not use of two for the M value.
d) Repeat the same steps until the n cycles are completed. So the answer is shown, in the last rows of A and B.

4.3 RADIX-4 BOOTH MULTIPLIER

The shortcomings of Radix-2 can get rid by Radix-4 in which it handle more than one bit of multiplier in each cycle. The modified Booth's algorithm starts by appending a zero to right of LSB of multiplier. This recoding scheme applied to a parallel multiplier halves the no. of partial products so the multiplication time & hardware requirement can get reduce.

4.3.1 RADIX-4 BOOTH ALGORITHM

Radix-4 Booth algorithm examines strings of three bits according to the following algorithm given below:

a) Increase the sign bit 1 position if required to verify that n is even.
b) The right side of the LSB of the multiplier adds with 0.
c) As per the value of all vectors, all Partial Product will be 0, +y, -y, +2y or -2y.

The values of y are comes negative due to taking the 2's complement. The multiplication of y performs by

left shifting y by one bit. As a result implementing of n-bit parallel multipliers, only n/2 partial products are created.

Table I: Radix-4 Modified Booth Algorithm for Odd Values of i

X(i)	X(i-1)	X(i-2)	y
0	0	0	+0
0	0	1	+y
0	1	0	+y
0	1	1	+2y
1	0	0	-2y
1	0	1	-y
1	1	0	-y
1	1	1	+0

4.3 WALLACE TREE MULTIPLIER

The Wallace tree multiplier is a high speed multiplier. The summing of the partial product bits in parallel using a tree of carry-save adders became generally known as the ”Wallace Tree (WT)”.

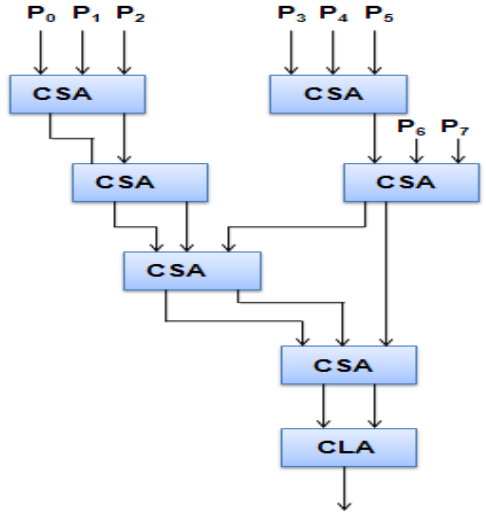

Fig. 8: Wallace Tree Multiplier

Three step processes are used to multiply two numbers.

a) Formation of bit products.
b) Reduction of the bit product matrix into a two row matrix by means of a carry save adder.
c) Summation of remaining two rows using a faster Carry Look Ahead Adder (CLA).

V. SIMULATIONS AND RESULT

In this paper we performed and analyzed high performance FIR filter by using low power adder and multiplier. All the circuits are designed and simulated using Xilinx and ModelSim SE-EE 5.4a software. The power calculation of all adder, multiplier and FIR filter is calculated by using XPower Estimator software.

Table II: Dynamic Power Consumption of Different Digital Adder

S.NO.	Digital Adder	Dynamic Power (mW)
1	Ripple Carry Adder	158
2	Carry Look Ahead Adder	162
3	Carry Select Adder	143
4	Carry Save Adder	140

Table III: Dynamic Power Consumption of Different Digital Multiplier

S.NO.	Digital Multiplier	Dynamic Power (mW)
1	Array Multiplier	130
2	Radix-2 Booth Multiplier	118
3	Radix-4 Booth Multiplier	76
4	Wallace Tree Multiplier	80

Table IV: Dynamic Power Consumption of Different FIR Filter

S.NO.	FIR Filter	Dynamic Power (mW) at 50 MHz
1	Proposed FIR Filter	208
2	Existing FIR Filter	232
3	FIR Filter (ref. 4)	228

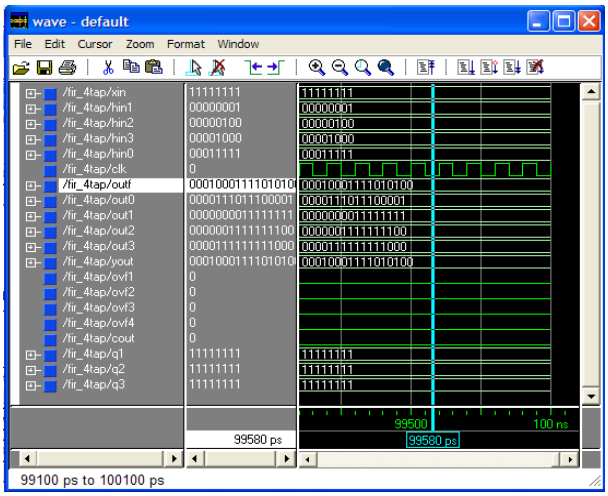

Fig 9: Simulation Results for Proposed FIR Filter

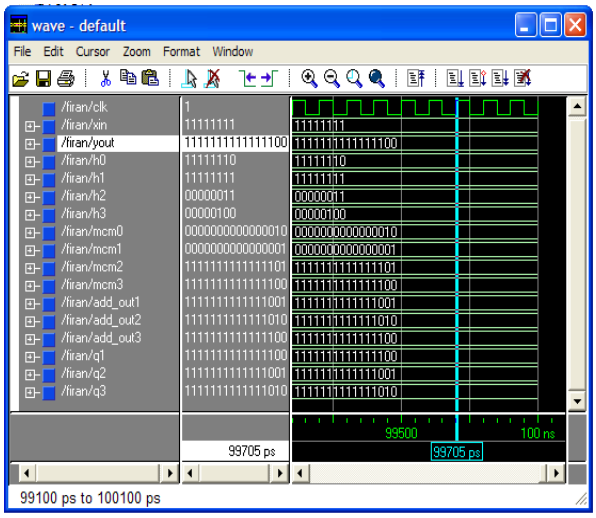

Fig. 10: Simulation Result for Existing FIR Filter

VI. CONCLUSION

Low power consumption is the most important criteria for the high performance DSP system. High performance system can be achieved by reduce its dynamic power that is the most important part of total power dissipation. Power dissipation in FIR filter has been much researched in recent years, due to the importance of the multiplication and addition arithmetic operation in wide are of DSP system. The research work presented in this dissertation has achieved good results and demonstrated the efficiency of high level optimization techniques. This report implements a high performance FIR filter using low power adder and multiplier. In this work we analyzed the different adder and multiplier on basis of their dynamic power dissipation. According to analysis result of adders and multipliers, we achieved carry save adder and radix4 multiplier is consuming low power among all adder and multiplier respectively. By using CSA and Radix 4 multiplier, we implemented the FIR filter and analyzed its power consumption. The performance curve of power dissipation by adders and multipliers was derived form analysis of different adders and multipliers. On the basis of power consumption result of proposed and existing FIR filter. The conclusion come out that proposed FIR filter is consume 10.36% power lesser than existing FIR Filter. So, according to result proposed FIR filter is the best for DSP system.

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